NEC

MOS INTEGRATED CIRCUIT

# μPD16602

## 312-OUTPUT TFT-LCD FULL COLOR DRIVER

The μPD16602 is a TFT-LCD source driver with full color display capability. It is ideal for 1024 × 768 pixel (XGA) class high definition displays. The internal circuit consists of 12 channels (4 × 3) of analog input pins, 12 channels of 16-bit shift registers and 312 channels of sample & hold circuits (2 latch type).

Analog display signals are sampled in 12 channels simultaneously by the sample & hold circuits and they are output in the next line. The output voltage of the sample & hold circuits is as great as 10.5 $V_{P-P}$ and maintains high accuracy with an output deviation of ±20 $mV_{MAX}$. Inputting analog display signals that been γ -processed in the previous stage signal processing circuit allows realization of a high definition 256-gray-scale-equivalent full color display without requiring line inversion.

### FEATURES

- 4 × 3 (RGB)-channel analog input allows display signal input wiring to be reduced.
- High dynamic range (10.0 $V_{P-PMIN.}$ $V_{DD2}$ = 11.0 V)
- High accuracy sample & hold circuits (output deviation; ±20 $mV_{MAX.}$, ±5.0 $mV_{TYP.}$)
- High-speed sampling frequency (for both analog and digital; $f_{max.}$ = 20 $MHz_{MIN.}$)
- Low power control (reduction of output buffer bias current) function on chip
  (operating power consumption; 82 $mW_{TYP.}$, $V_{DD2}$ = 12.5 V)
- Bi-directional data store function on chip
- Corresponding to high-density mounting (slim TCP)

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPD16602N-××× | TCP |

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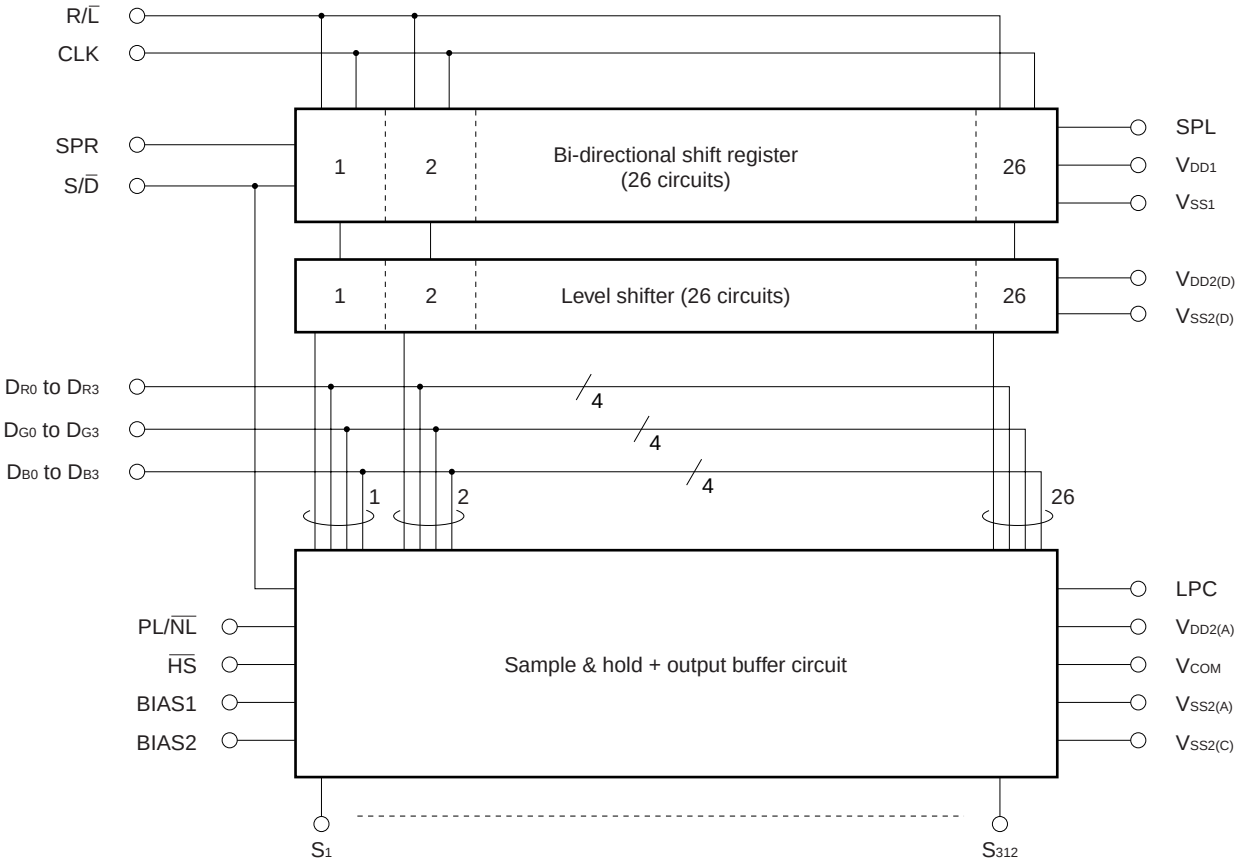
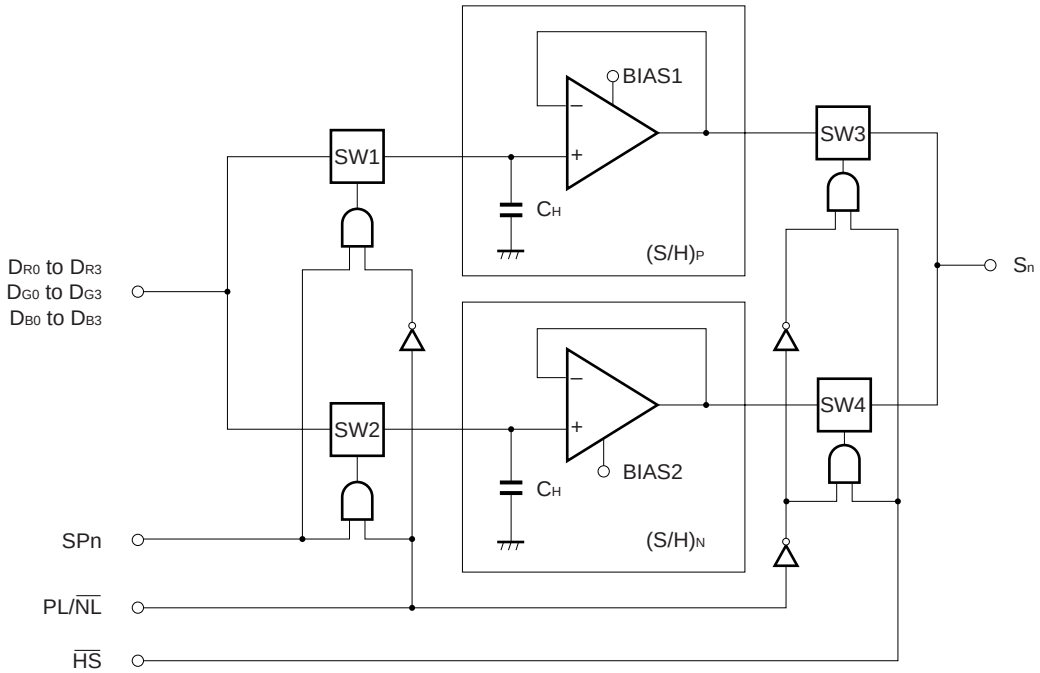
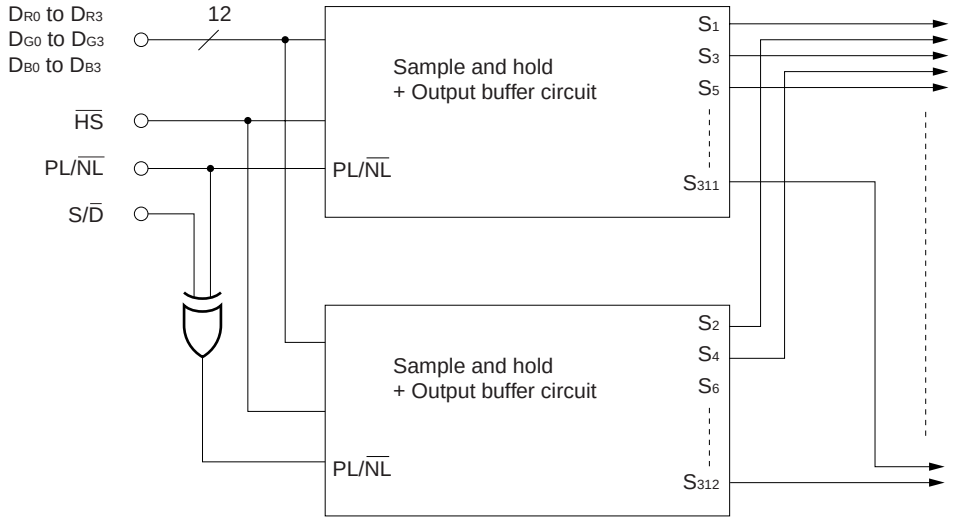
## 1. BLOCK DIAGRAM



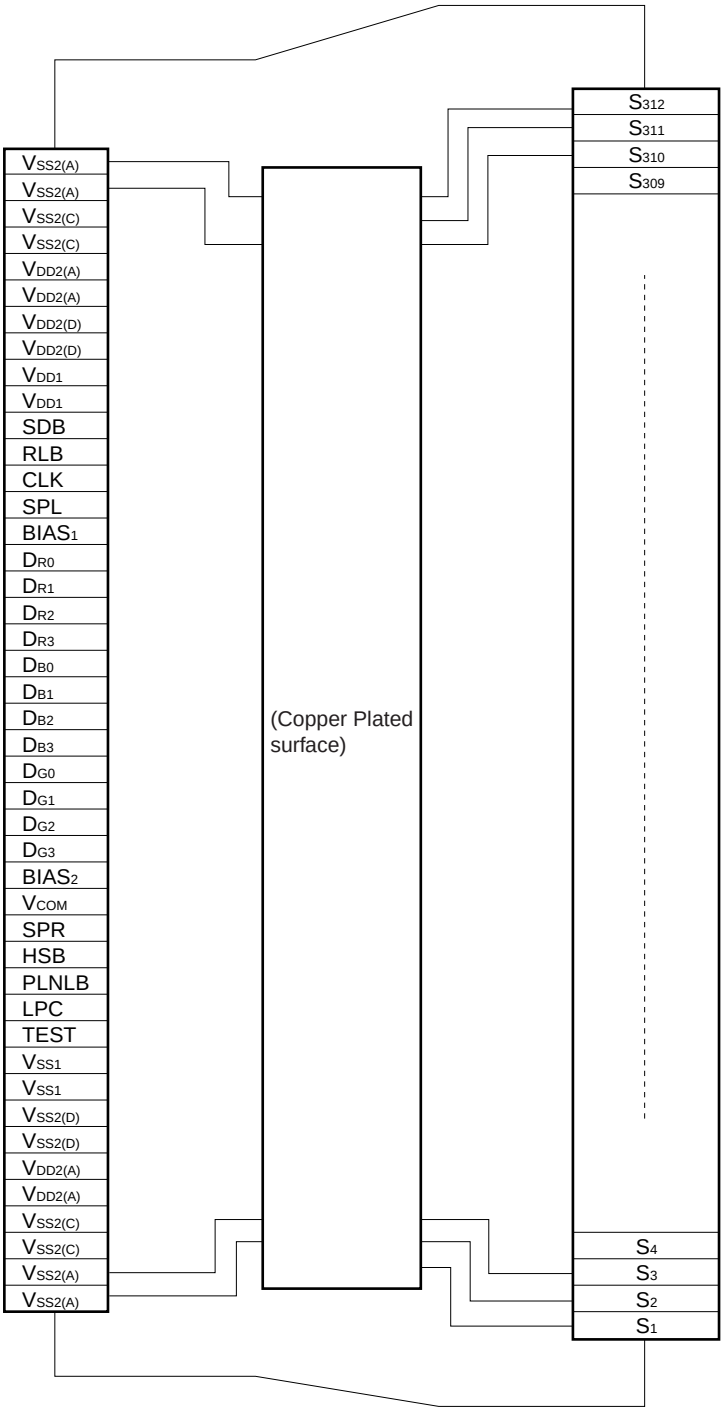

### SAMPLE & HOLD + OUTPUT BUFFER CIRCUIT 1



## SAMPLE & HOLD + OUTPUT BUFFER CIRCUIT 2



## 2. PIN CONFIGURATION



## 3. PIN DESCRIPTION

| Pin Symbol | Pin Name | Description |
|---|---|---|
| $S_1$ to $S_{312}$ | Driver outputs | Output pins for sampled analog image signals. When driven with $V_{DD2}$ = 12.5 V, a 11.5 $V_{P-P}$ analog voltage whose input/output characteristic is gain 1 is output. |
| CLK | Clock input | This pin reads the start pulse at the rising of CLK and starts sampling of analog display signals in 12 channels simultaneously. The active edges of CLK are all rising edges. |
| $D_{R0}$ to $D_{R3}$<br>$D_{G0}$ to $D_{G3}$<br>$D_{B0}$ to $D_{B3}$ | Analog display signal inputs | Analog image signal input pins. Please input analog display signals by inverting the polarity for each display line. |
| R/$\overline{L}$ | Shift direction switching input | The shift direction of the shift register is as follows.<br>R/$\overline{L}$ = H (right shift) ; SPR input, $S_1 \rightarrow S_{312}$, SPL output<br>R/$\overline{L}$ = L (left shift) ; SPL input, $S_{312} \rightarrow S_1$, SPR output |
| SPR | Start pulse input/ output | R/$\overline{L}$ = H (right shift) ; start pulse input pin<br>R/$\overline{L}$ = L (left shift) ; start pulse output pin |
| SPL | Start pulse input/ output | R/$\overline{L}$ = H (right shift) ; start pulse output pin<br>R/$\overline{L}$ = L (left shift) ; start pulse input pin |
| PL/$\overline{NL}$ Note | Polarity inversion input | S/$\overline{D}$ = L; When PL/$\overline{NL}$ = H, Both odd number pin and even number pin samples negative analog display signals and outputs positive analog signals from the driver output.<br>When PL/$\overline{NL}$ = L, Both odd number pin and even number pin samples positive analog display signals and outputs negative analog signals from the driver output.<br>S/$\overline{D}$ = H; When PL/$\overline{NL}$ = H, Odd number pin samples negative analog display signals and outputs positive analog signals from the driver output. Even number pin samples positive analog display signals and outputs negative analog signals from the driver output.<br>When PL/$\overline{NL}$ = L, Odd number pin samples positive analog display signals and outputs negative analog signals from the driver output. Even number pin samples negative analog display signals and outputs positive analog signals from the driver output. |
| S/$\overline{D}$ | Arrangement switching input | S/$\overline{D}$ = H; Complying with one side arrangement dot inverting.<br>S/$\overline{D}$ = L; Complying with both sides arrangement dot inverting. |
| $\overline{HS}$ Note | Horizontal synchronous input | This pin shuts off the output at the falling edge and then outputs analog display signals at the rising. When $\overline{HS}$ = L, after the driver output pin goes to high impedance this pin switches PL/$\overline{NL}$ and resets the internal hold capacity and output buffer to the $V_{COM}$ level. |
| LPC | Low power control input | This pin shuts off the output buffer low current supply and increases the output impedance. The LPC = "H" mode allows the static current consumption to be reduced by approximately 20 %. |
| $BIAS_1$<br>$BIAS_2$ | Bias voltage inputs | These pins control the current consumption of the output buffer by applying a stabilized external power supply. |
| $V_{DD1}$ | Logic power supply | 3.3 V ±0.3 V |
| $V_{DD2(D)}$ | Driver power supply | 13.5 $V_{MAX.}$ |
| $V_{DD2(A)}$ | Driver power supply | 13.5 $V_{MAX.}$ |
| $V_{COM}$ | Common power supply | This pin applies the intermediate voltage of a stable LCD drive voltage from a voltage follower, etc. |
| $V_{SS1}$ | Logic ground | Logic ground |
| $V_{SS2(D)}$ | Driver ground | High voltage block (level shifter) |
| $V_{SS2(A)}$ | Driver ground | High voltage block (output buffer) |
| $V_{SS2(C)}$ | Driver ground | High voltage block (sample & hold) |
| TEST | Test pin | "L" or left open |

**Note** Sample & hold operation and reset operation of the output buffer capacitance and $V_{COM}$ level are performed by the PL/$\overline{NL}$ and $\overline{HS}$ logic.

## 4. NOTES ON USE

(1) In order to prevent latch up breakdown, power should be applied in the order of:
$V_{DD1}$ → logic input → $V_{DD2(D),\,(A)}$ → $V_{BIAS1,2}$, $V_{COM}$ → analog display signal input, and turned off in the reverse order.
This order should also be observed in transition periods.

(2) $V_{SS1}$, $V_{SS2(D)}$, $V_{SS2(A)}$ and $V_{SS2(C)}$ are connected in the diffusion layer, but also be sure to connect them externally.
Do not share the sample & hold ground $V_{SS2(C)}$ with other ground wiring on the mount board, but connect it to the edge to the signal board. There is a possibility of high-voltage or logic type noise being superimposed onto the sample & hold circuit, damaging the analog characteristics (output deviation, etc.).

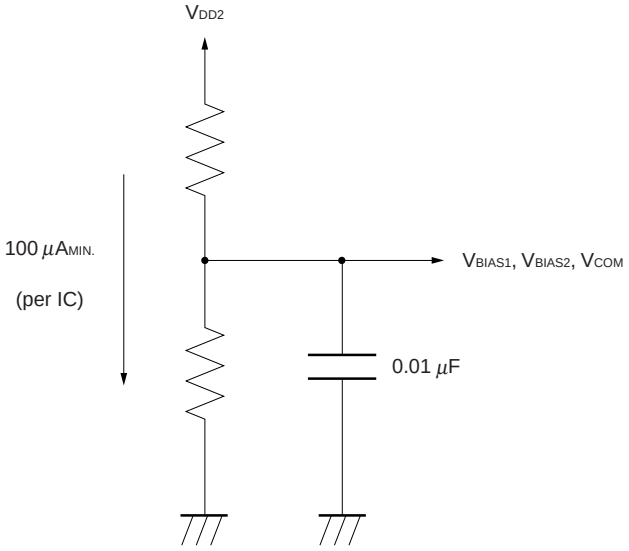
(3) Likewise, to prevent the sample & hold characteristics from deteriorating, insert a bypass capacitor of 0.1 μF between $V_{DD1}$ and $V_{SS1}$, and approximately 0.1 μF between $V_{DD2(D),\,(A)}$ and $V_{SS2(D),\,(A)}$. An unstable power supply may cause a driver through current, preventing the output range of the output buffer from being sufficiently secured. Therefore, determine the capacitance of the bypass capacitor after a thorough evaluation.

(4) When LPC = "H", stable current supply of the output buffer may be shut off, which will impede normal negative feedback, and when the LCD panel load is small, the output voltage may become abnormal.
Normal operation is assured with approximately 10 kΩ + 50 pF, but when the time constant is smaller than this, please set LPC = "L".

(5) Data input/output relationship
As shown below, irrespective of right shift and left shift.

| Output | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | | $S_{309}$ | $S_{310}$ | $S_{311}$ | $S_{312}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Data | $D_{R0}$ | $D_{B0}$ | $D_{G0}$ | $D_{R1}$ | $D_{B1}$ | $D_{G1}$ | | $D_{G2}$ | $D_{R3}$ | $D_{B3}$ | $D_{G3}$ |

(6) Bias control method
Externally applying a voltage to pins $BIAS_1$ and $BIAS_2$ can control the output buffer current consumption. In this case, the analog characteristics (output deviation, driving capability, response speed, etc.) will not change. Please refer to the configuration in the figure below for the actual circuit. Also refer to the same configuration for the $V_{COM}$ voltage input circuit. Current per driver IC is as follws.



## 5. FUNCTIONAL DESCRIPTION

### (1) Input Specification of the analog display signal (n = 0 to 25, R/$\overline{L}$ = "H" or "L")

| | | Display signal input terminal/Output terminal | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| S/$\overline{D}$ | PL/$\overline{NL}$ | $D_{R0}$ $S_{12n}$ + 1 | $D_{B0}$ $S_{12n}$ + 2 | $D_{G0}$ $S_{12n}$ + 3 | $D_{R1}$ $S_{12n}$ + 4 | – – – | $D_{G2}$ $S_{12n}$ + 9 | $D_{R3}$ $S_{12n}$ + 10 | $D_{B3}$ $S_{12n}$ + 11 | $D_{G3}$ $S_{12n}$ + 12 |
| H | H | (–) | (+) | (–) | (+) | – – – | (–) | (+) | (–) | (+) |
| | L | (+) | (–) | (+) | (–) | – – – | (+) | (–) | (+) | (–) |
| L | H | (–) | (–) | (–) | (–) | – – – | (–) | (–) | (–) | (–) |
| | L | (+) | (+) | (+) | (+) | – – – | (+) | (+) | (+) | (+) |

(+) : Please input the positive analog input signal.

(–) : Please input the negative analog input signal.

### (2) Output Specification of the analog display signal

- Single Bank Arrangement for dot inversion (S/$\overline{D}$ = "H")

  Polarity of the output voltage

| Line No. | PL/$\overline{NL}$ | $S_1$ ($D_{R0}$) | $S_2$ ($D_{R0}$) | $S_3$ ($D_{G0}$) | $S_4$ ($D_{R1}$) | $S_5$ ($D_{B1}$) | $S_6$ ($D_{G1}$) | $S_7$ ($D_{R2}$) | ··· |
|---|---|---|---|---|---|---|---|---|---|
| 1 | H | (+) | (–) | (+) | (–) | (+) | (–) | (+) | ··· |
| 2 | L | (–) | (+) | (–) | (+) | (–) | (+) | (–) | ··· |
| 3 | H | (+) | (–) | (+) | (–) | (+) | (–) | (+) | ··· |
| 4 | L | (–) | (+) | (–) | (+) | (–) | (+) | (–) | ··· |
| 5 | H | (+) | (–) | (+) | (–) | (+) | (–) | (+) | ··· |

(+) : Positive analog output (Negative line sampling), (–) : Negative analog output (Positive line sampling)

- Dual Bank Arrangement for dot inversion (S/$\overline{D}$ = "L")

  Polarity of the each output voltage

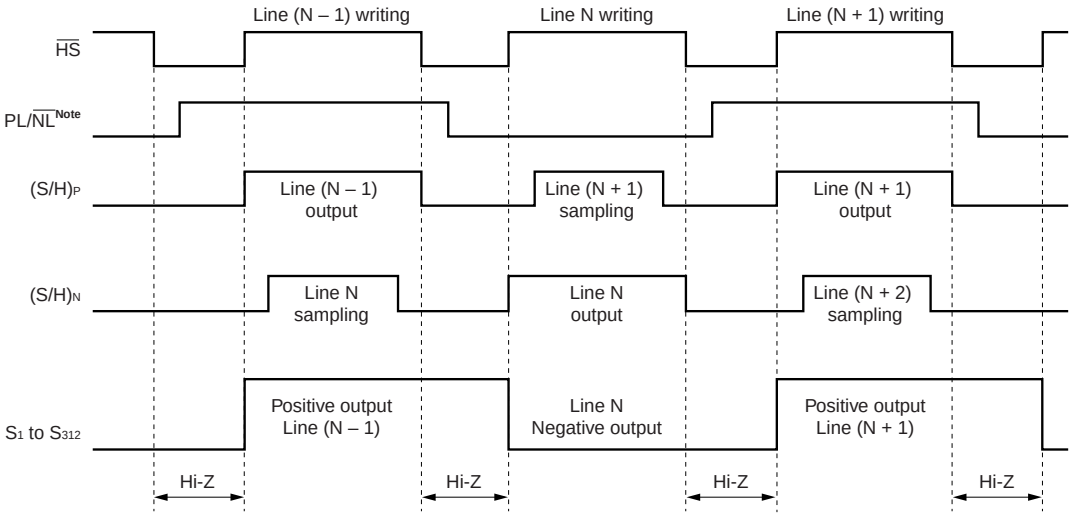
| | Input signal polarity | | Output Polarity of the upper driver IC's | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Line No. | PL/$\overline{NL}$ | | $S_1$ ($D_{R0}$) | | $S_2$ ($D_{B0}$) | | $S_3$ ($D_{G0}$) | | $S_4$ ($D_{R1}$) | |
| | Upper side | Lower side | | | | | | | | |
| 1 | H | L | (+) | (–) | (+) | (–) | (+) | (–) | (+) | (–) |
| 2 | L | H | (–) | (+) | (–) | (+) | (–) | (+) | (–) | (+) |
| 3 | H | L | (+) | (–) | (+) | (–) | (+) | (–) | (+) | (–) |
| 4 | L | H | (–) | (+) | (–) | (+) | (–) | (+) | (–) | (+) |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 767 | H | L | (+) | (–) | (+) | (–) | (+) | (–) | (+) | (–) |
| 768 | L | H | (–) | (+) | (–) | (+) | (–) | (+) | (–) | (+) |
| | | | | $S_{312}$' ($D_{G3}$') | | $S_{311}$' ($D_{B3}$') | | $S_{310}$' ($D_{R3}$') | | $S_{309}$' ($D_{G2}$') |
| | | | Output polarity of the lower driver IC's | | | | | | | |

$S_n$ : Output voltage of the upper side driver, (+) : Positive output of the upper side driver

$S_{n'}$ : Output voltage of the lower side driver, (–) : Negative output of the lower side driver

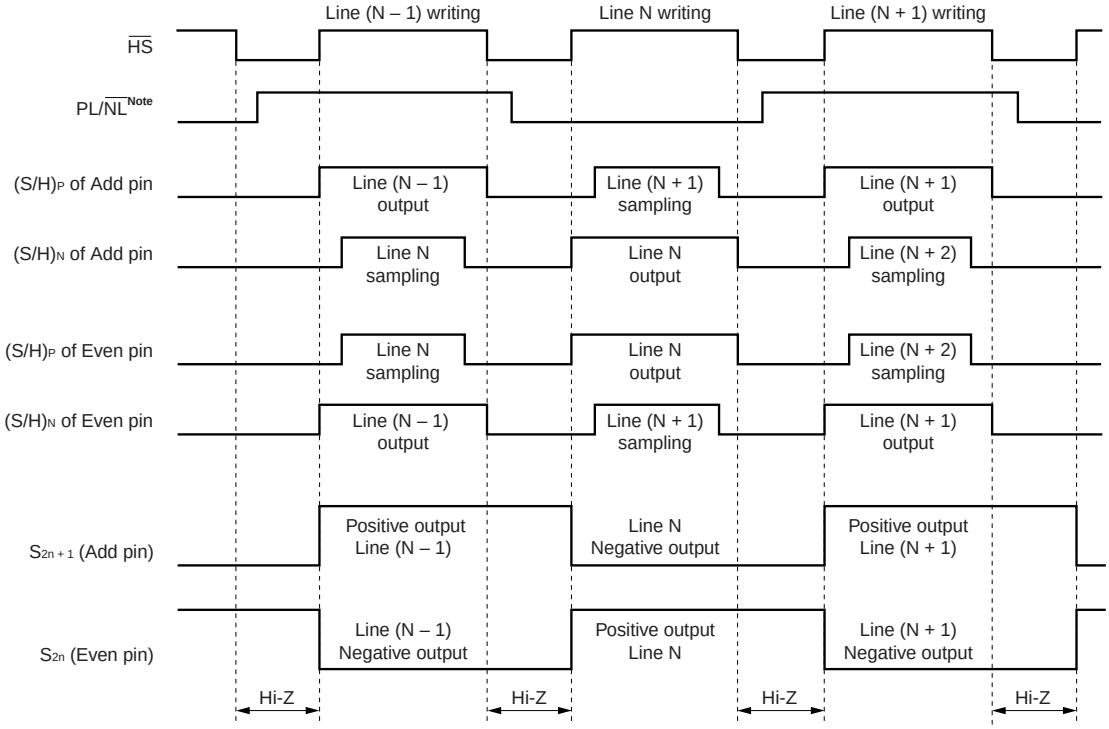
### (3) Sampling and hold timing (R/$\overline{L}$ = "L")

**S/$\overline{D}$ = "L" (Dual Bank Arrangement)**



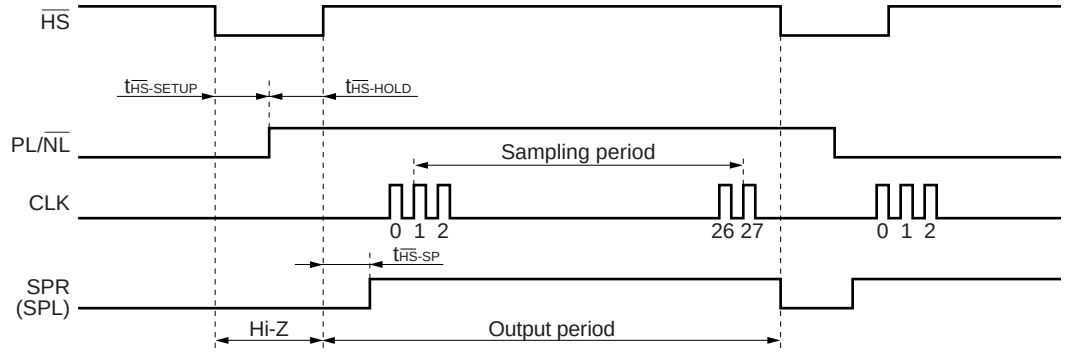

**Note** PL/$\overline{NL}$ = H; input negative analog display signal.
PL/$\overline{NL}$ = L; input positive analog display signal.

**S/$\overline{D}$ = "H" (Single Bank Arrangement)**




**Note** Odd number pin PL/$\overline{NL}$ = H; input negative analog display signal.
PL/$\overline{NL}$ = L; input positive analog display signal.
Even number pin PL/$\overline{NL}$ = H; input positive analog display signal.
PL/$\overline{NL}$ = L; input negative analog display signal.

**(4) Relatonship with $\overline{HS}$ and PL/$\overline{NL}$**

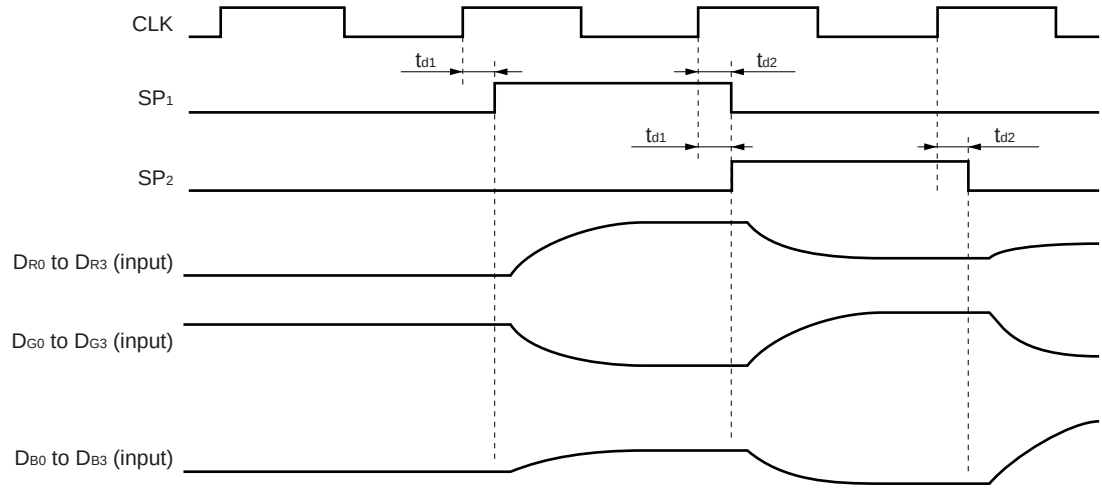



**Caution $\overline{HS}$ and PL/$\overline{NL}$ edges have no relationship with clock timing.**

| Timing Item | Symbol | Description |
|---|---|---|
| Horizontal synchronization setup time | $t_{\overline{HS}\text{-SETUP}}$ | Setup time of PL/$\overline{NL}$ signal with respect to $\overline{HS}$.<br>Secure 50 ns$_{MIN.}$ at least. |
| Horizontal synchronization hold time | $t_{\overline{HS}\text{-HOLD}}$ | PL/$\overline{NL}$ hold time. Secure 250 ns$_{MIN.}$ at least.<br>The hold capacitance at this time is at common potential $V_{COM}$, but the output buffer does not reach $V_{COM}$, and therefore sampling is not possible. |
| Sampling start time | $t_{\overline{HS}\text{-SP}}$ | Time for the output buffer to reach $V_{COM}$ (reset level).<br>Secure 1.0 $\mu$s$_{MIN}$ at least. Sampling is possible at this time.<br>Input the start pulse at this time. |

These characteristics are specified by load constants of 50 kΩ + 100 pF.

**(5) Internal sampling delay**

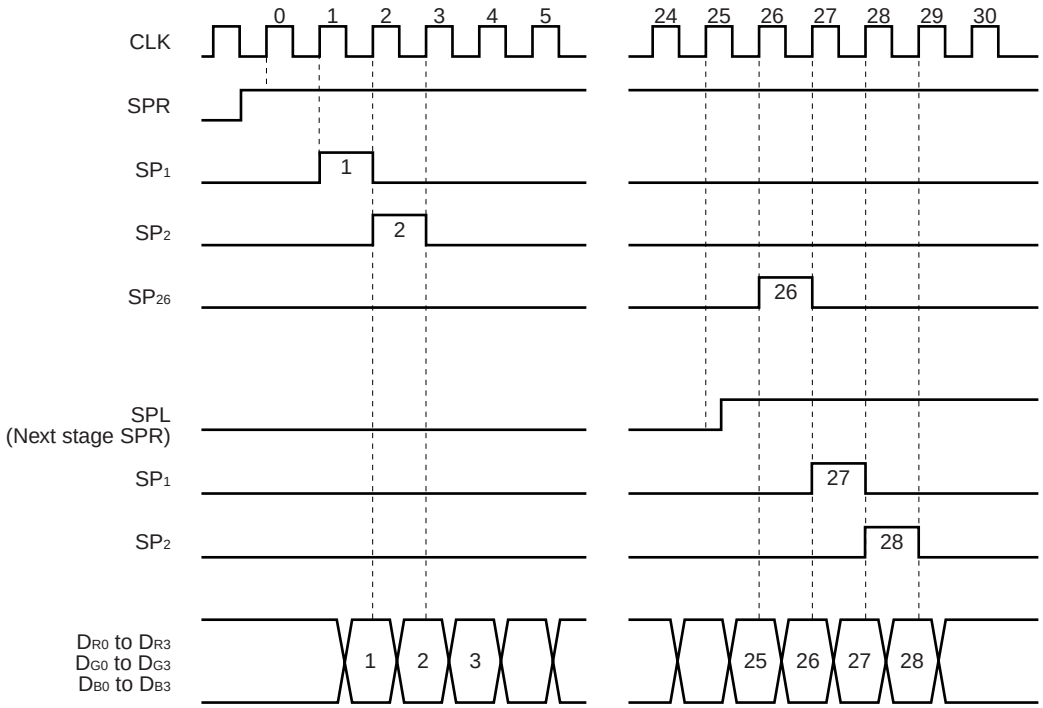



| Timing Duration | Symbol | Description |
|---|---|---|
| CLK-sampling pulse delay | $t_{d1}$ | Delay time between CLK signal and rising edge of internal sampling pulse SPn.<br>Input an analog image signal with a timing difference of $t_{d1}$ in order to secure a sufficient sampling period. |
| Sampling pulse-CLK delay | $t_{d2}$ | Delay time between CLK signal and falling edge of internal sampling pulse. |

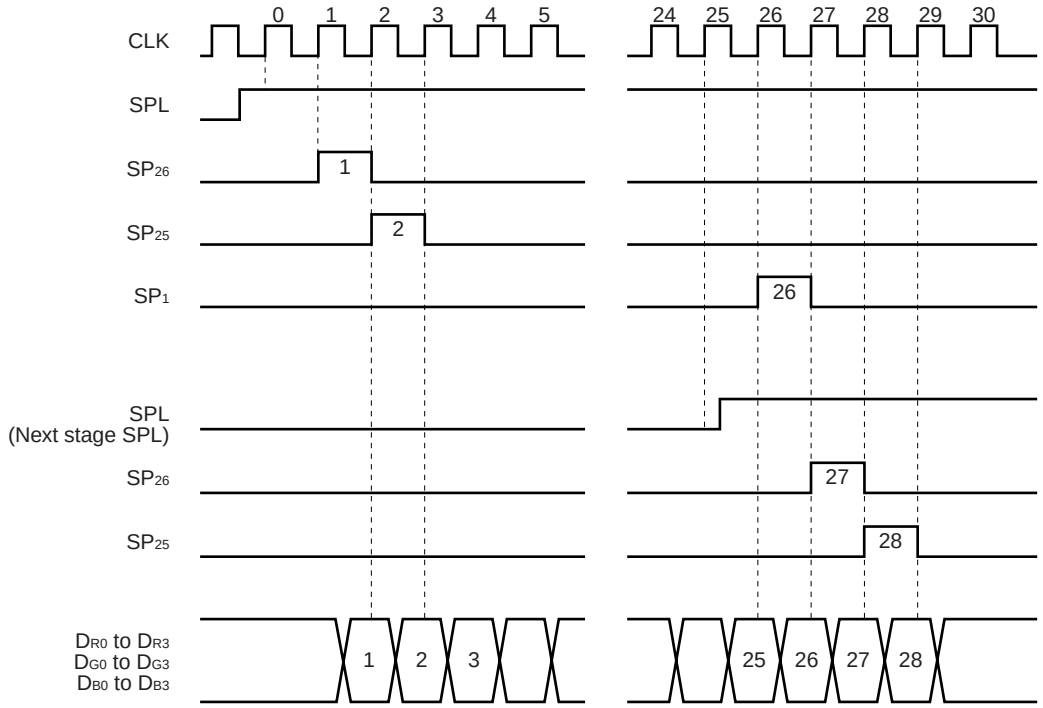
$t_{d1}$ is 22 ±5 ns and $t_{d2}$ is 14 ±5 ns (these are not guaranteed values).

### (6) Cascade timing

R/$\overline{L}$ = H (right shift)




R/$\overline{L}$ = L (left shift)



## 6. ELECTRIC SPECIFICATION

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C, $V_{SS(D),(A),(C)}$ = 0 V)

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Logic supply voltage | $V_{DD1}$ | –0.5 to +6.5 | V |
| Logic input voltage | $V_{IN}$ | –0.5 to $V_{DD1}$ +0.5 | V |
| Logic output voltage | $V_{O1}$ | –0.5 to $V_{DD1}$ +0.5 | V |
| Driver supply voltage | $V_{DD2\ (D),\ (A)}$ | –0.5 to +15 | V |
| Display signal input voltage | $V_{IN\ (A)}$ | –0.5 to $V_{DD2}$ +0.5 | V |
| Driver output voltage | $V_{O2}$ | –0.5 to $V_{DD2}$ +0.5 | V |
| Driver output current | $I_{O2}$ | ±10 | mA |
| Operating temperature range | $T_A$ | –10 to +75 | °C |
| Storage temperature range | $T_{stg}$ | –40 to +125 | °C |

### RECOMMENDED OPERATING RANGE ($T_A$ = –10 to 75°C, $V_{SS}$ = 0 V)

| Item | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Logic supply voltage | $V_{DD1}$ | 3.0 | 3.3 | 3.6 | V |
| High-level input voltage | $V_{IH}$ | 0.7 $V_{DD1}$ | | | V |
| Low-level input voltage | $V_{IL}$ | | | 0.3 $V_{DD1}$ | V |
| Driver supply voltage | $V_{DD2}$ | 11.0 | 12.5 | 13.5 | V |
| Display signal input | $V_{IN\ (A)}$ | $V_{SS}$ +0.5 | | $V_{DD2}$ –0.5 | V |
| Driver output voltage | $V_O$ | $V_{SS}$ +0.5 | | $V_{DD2}$ –0.5 | V |
| Bias current | $I_{BIAS1,\ 2}$ | 100 | | | μA |
| Bias voltage | $V_{BIAS1}$ | $V_{SS}$ +4.5 | $V_{SS}$ +5.0 | $V_{SS}$ +5.5 | V |
| | $V_{BIAS2}$ | $V_{DD2}$ –7.5 | $V_{DD2}$ –7.0 | $V_{DD2}$ –6.5 | V |

**ELECTRICAL SPECIFICATIONS ($T_A$ = –10 to 75°C, $V_{DD1}$ = 3.3 V ±0.3 V, $V_{DD2}$ = 12.5 $^{+1.0}_{-1.5}$ V, $V_{SS}$ = 0 V)**

| Item | Symbol | Condition | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-level output voltage | $V_{OH}$ | Logic, $I_{OH1}$ = 0 mA | | $V_{DD1}$ –0.1 | | | V |
| Low-level output voltage | $V_{OL}$ | Logic, $I_{OL1}$ = 0 mA | | | | 0.1 | V |
| Input leakage current | $I_{iL}$ | $V_i$ = $V_{DD1}$, $V_{SS1}$ | | | | ±10 | μA |
| Driver output current (black level) | $I_{OH11}$ | PL/$\overline{NL}$ = H (source) | $V_R$ = $V_G$ = $V_B$ = 11 V | | | –0.3 | mA |
| Driver output current (white level) | $I_{OH12}$ | $V_O$ = 3.0 V | $V_R$ = $V_G$ = $V_B$ = 7 V | | | –0.3 | mA |
| Driver output current (white level) | $I_{OH21}$ | PL/$\overline{NL}$ = L (sink) | $V_R$ = $V_G$ = $V_B$ = 5 V | 0.3 | | | mA |
| Driver output current (black level) | $I_{OH22}$ | $V_O$ = 9.0 V | $V_R$ = $V_G$ = $V_B$ = 1 V | 0.3 | | | mA |
| Output off leakage current | $I_{OFF}$ | $V_{O2}$ = $V_{DD2}$, $V_{SS}$ | | | | ±1 | μA |
| Dynamic current consumption | $I_{DD12}$ | $V_{DD1}$, $f_{CLK}$ = 20 MHz | | | 0.3 | 0.8 | mA |
| | $I_{DD22}$ | $V_{DD2}$, $f_{\overline{HS}}$ = 66 kHz, LPC = L, No load | | | 9.5 | 15 | mA |
| | | $V_{DD2}$, $f_{\overline{HS}}$ = 66 kHz, LPC = H, No load | | | 6.5 | 13 | mA |
| Static current consumption | $I_{DD21}$ | $V_{DD2}$, No load<br>$f_{\overline{HS}}$ = 66 kHz, LPC = L | | | 9.0 | 14 | mA |
| | | $V_{DD2}$, No load<br>$f_{\overline{HS}}$ = 66 kHz, LPC = H | | | 6.0 | 12 | mA |
| Output deviation[Note] | $\Delta V_O$ | $V_R$ = $V_G$ = $V_B$ = 7 to 11 V, PL/$\overline{NL}$ = H | | | ±5.0 | ±20 | mV |
| | | $V_R$ = $V_G$ = $V_B$ = 1 to 5 V, PL/$\overline{NL}$ = L | | | ±5.0 | ±20 | mV |

**Note** The “deviation” indicates the minimum and maximum values in the driver output voltage distribution in the chip.

**SWITCHING CHARACTERISTICS ($T_A$ = –10 to +75°C, $V_{DD1}$ = 3.3 V ±0.3 V, $V_{DD2}$ =12.5 $^{+1.0}_{-1.5}$ V, $V_{SS}$ = 0 V)**

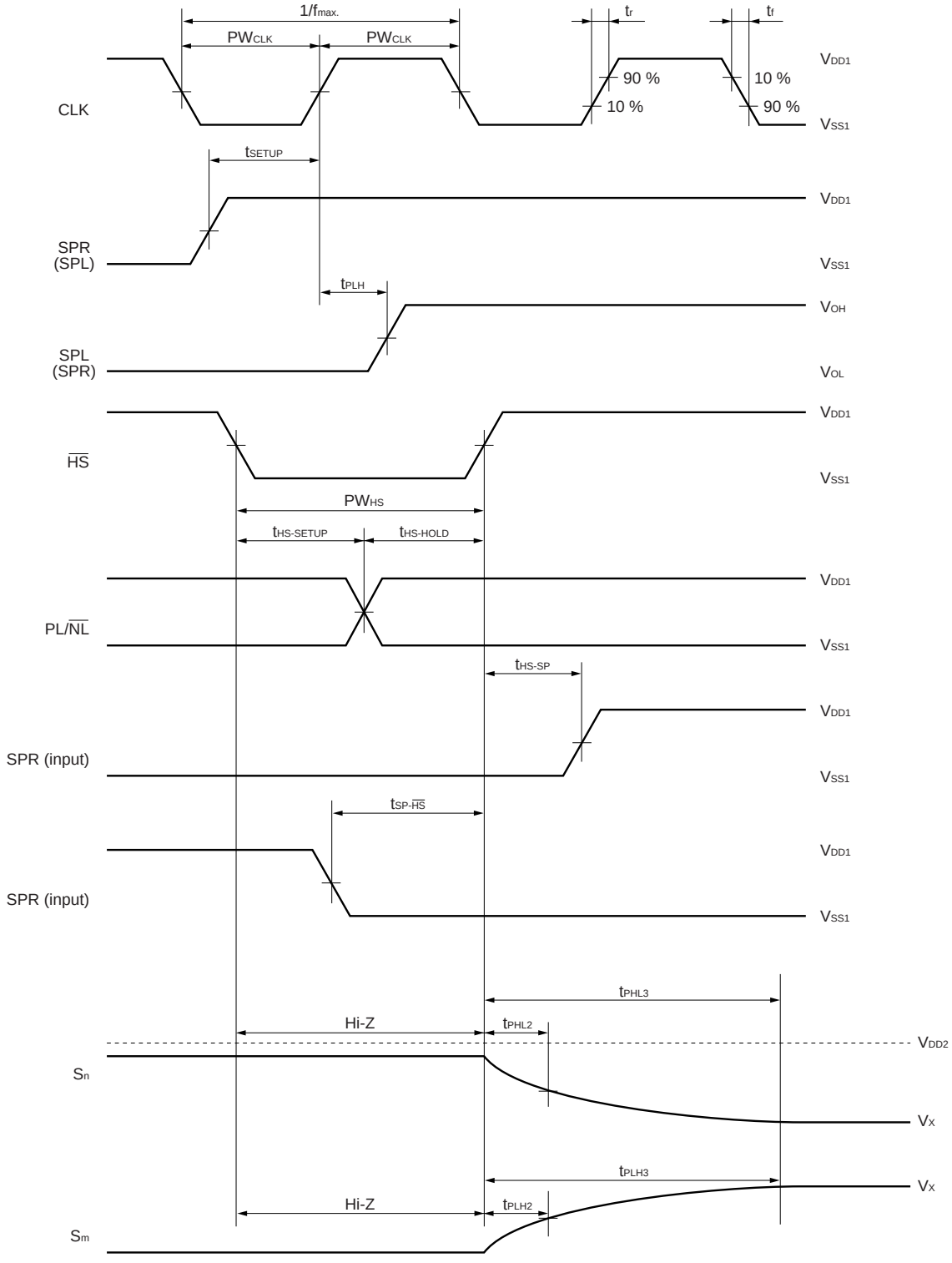
| Item | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Start pulse output delay tIme | $t_{PLH1}$ | $C_L$ = 20 pF | 12 | 20 | 40 | ns |
| Driver output delay time | $t_{PHL2}$ | $C_L$ = 50 pF, R = 50 kΩ | | 6.75 | 11 | μs |
| | $t_{PHL3}$ | | | 13.5 | 17 | μs |
| | $t_{PLH2}$ | | | 6.75 | 11 | μs |
| | $t_{PLH3}$ | | | 13.5 | 17 | μs |
| Input capacitance | $C_{i1}$ | Logic except for SPR (SPL), $T_A$ = 25°C | | 7 | 10 | pF |
| | $C_{i2}$ | SPR (SPL), $T_A$ = 25°C | | 10 | 15 | pF |
| | $C_{i3}$ | Display signal input pin | | 20 | | pF |
| Maximum clock frequency | $f_{max.}$ | | 20 | | | MHz |

**TIMING REQUIREMENT ($T_A$ = –10 to +75°C, $V_{DD1}$ = 3.3 V ±0.3 V, $V_{SS}$ = 0 V, $t_r$ = $t_f$ = 5 ns)**

| Item | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Clock pulse width | $PW_{CLK}$ | Duty = 50 % | 25 | | | ns |
| Horizontal synchronous signal pulse width | $PW_{\overline{HS}}$ | | 300 | | | ns |
| Start pulse setup time | $t_{SETUP}$ | | 10 | | | ns |
| CLK-sampling pulse delay time | $t_{d1}$ | | | 15 | | ns |
| Sampling pulse-CLK delay time | $t_{d2}$ | | | 15 | | ns |
| Horizontal synchronous signal setup time | $t_{\overline{HS}\text{-SETUP}}$ | | 50 | | | ns |
| Horizontal synchronous signal hold time | $t_{\overline{HS}\text{-HOLD}}$ | | 250 | | | ns |
| $\overline{HS}$-start pulse time | $t_{\overline{HS}\text{-SP}}$ | | 1.0 | | | μs |
| Start pulse-$\overline{HS}$ time | $t_{SP\text{-}\overline{HS}}$ | | 10 | | | ns |

**SWITCHING CHARACTERISTICS (R/$\overline{L}$ = H)** Items in ( ) apply when R/$\overline{L}$ = L.

Unless otherwise specified, the input levels are all set to 0.5 $V_{DD1}$




$V_X$ refers to the final output voltage, $t_{PLH2}$ and $t_{PHL2}$ refer to the time required to an output precision level of 10 % (0.1 $V_X$); and $t_{PLH3}$ and $t_{PHL3}$ refer to the time required to reach an output precision level of 6 bits.

## RECOMMENDED MOUNTING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

| Mounting Condition | Mounting Method | Condition |
|---|---|---|
| Thermocompression | Soldering | Heating tool 300 to 350°C, heating for 2 to 3 seconds; pressure 100 g (per solder) |
| | ACF (Adhesive Conductive Film) | Temporary bonding 70 to 100°C; pressure 3 to 8 kg/cm$^2$; time 3 to 5 secs.<br>Real bonding 165 to 180°C; pressure 25 to 45 kg/cm$^2$, time 30 to 40 secs. (When using the anisotropic conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.) |

**Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.**

**Reference**

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)

Quality Grades on NEC Semiconductor Devices (C11531E)